UNIMORE
UNIVERSITÀ DEGLI STUDI DI MODENA E REGGIO EMILIA

Thursday May, 15th, 2025, 11:00-13:00

c/o Building MO27, Room Master

Engrs. E.Temporiti, E.Monaco, G.Gira
with Marvell (Pavia, Italy)
will held a seminar entitled

"Marvell powering the AI era: A 5nm 800Gb/s Transceiver for PAM-4 Optical Direct-Detection applications"

As part of:

- Bachelor's degree programme in Electronics Engineering
- Master's degree programme in Electronics Engineering
- Ph.D. in Information and Communication Technologies

Abstract: Marvell, a fabless semiconductor company headquartered in Silicon Valley, offers a comprehensive portfolio of data infrastructure solutions for the AI landscape. The Marvell team in Pavia is specialized in the design and validation of high-speed transceivers in the most advanced technology nodes.
In this seminar an 8x100Gb/s electro-optical transceiver for PAM-4 optical interconnects in 5nm FinFET technology will be presented. The transceiver, currently in mass production, comes with three transmitter variants to drive various optical devices. The receivers are DSP based, featuring an analog front end with a Variable Gain Amplifier (VGA) and an ADC. The presentation will introduce the application and an overview of the architecture and key components.

Enrico Temporiti: received his Laurea degree in Electronic Eng. from the University of Pavia in 1999, in collaboration with Alcatel. In 2000 he joined STMicroelectronics, where he held various roles in advanced R&D, strategic planning and product development. Since 2019 he has been with Marvell Technology (formerly Inphi and eSilicon), where he currently serves as Senior Director of Engineering, leading the development of electrical and optical PHYs.

Enrico Monaco: born in Carpi, Italy, in 1983, earned his MS and Ph.D. degrees in Electrical Eng. from the University of Modena, Italy, in 2008 and 2012, respectively. From 2011 to 2017, he worked as a Design Engineer in the Serial Interfaces Group at "Studio di Microelettronica" in Pavia, specializing in analog Serializer/Deserializer (SerDes) technology. Since 2018, he has been a Senior Principal Eng. at Marvell Technology in Pavia. His work focuses on high-speed analog-to-digital converters (ADCs) and analog front ends for wireline interfaces. In 2009, he received the AMD/CICC Student Scholarship Award at the Custom Integrated Circuits Conference (CICC).

Gabriele Gira: born in Pavullo Nel Frignano (MO), Italy, in 1995, obtained his BS and MS in Electronic Eng. at the University of Modena & Reggio-Emilia in April 2018 and April 2021, respectively. After a period of one year and a half in a start-up based in Modena working as Analog IC Designer, he joined Marvell Technology in Pavia, Italy, in January 2023, where he currently holds the position of Analog Mixed-Signal Design, Staff Eng. in the TX design team. In this role, he works for the design of TX front-end for cutting-edge high-speed SerDes in FinFET technology.